LISTING OF AND AMENDMENTS TO CLAIMS:

1. (currently amended) An apparatus ~~Apparatus~~ ~~(2)~~ for determining the quality of a digital signal ~~(S)~~, comprising

a sampler ~~(10)~~ using clock cycles ~~(CLK)~~ for sampling the digital signal ~~(S)~~ with a number n of samples per defined pulse width, whereby $n \geqq 1$;

an edge detector ~~(20)~~ for detecting an edge of a pulse of the sampled digital signal;

a counter ~~(30)~~ for counting the clock cycles between edges detected by the edge detector; ~~and~~

a deviation detector ~~(40)~~ being able to compare the counted clock cycles ~~(EEC)~~ with a prestored reference-value ~~(EEC_n)~~ in order to provide a deviation value ~~(RJ)~~ as a measure for the instantaneous quality of the digital signal ~~(S)~~; and

an absolute-value limiter unit for generating an absolute deviation value in response to the deviation value and a storage latch for storing the absolute deviation value.

2. (canceled)

3. (original) Apparatus according to claim 1, comprising a leaky integrator (50) for generating a signal quality measure (J) in response to the absolute deviation value (PJ).

4. (original) Apparatus according to claim 3, wherein the leaky integrator (50) has a leak factor β having a power-of-two value of the form 2^{-m} with $m > 0$ such that β is in the range $0 < \beta \leqslant 1$.

5. (original) Apparatus according to claim 1, wherein the edge detector (20) bases edge detection on a first sample value and at least one second sample value.

6. (original) Apparatus according to claim 1, wherein the counter (30) comprises an up-counter, preferably a modulo N counter, where N is an integer number.

7. (original) Apparatus according to claim 1, wherein the deviation detector (40) comprises a comparator (44) that provides a positive or negative deviation value (RJ).

8. (original) Apparatus according to claim 1, wherein the digital signal (S) is encoded by a pulse modulation, preferably a Pulse Position Modulation (PPM), and wherein the digital signal (S) represents data carried in frames comprising at least a header field which contains a preamble and a data field.

9. (original) Apparatus according to claim 8, wherein the

quality of the digital signal (S) is determinable within the preamble.

10. (currently amended) Apparatus according to claim 1, wherein the digital signal (S) comprises an infrared signal~~, preferably a 4-PPM signal~~.

11. (original) Apparatus according to claim 1, wherein the digital signal (S) comprises noisy signals containing no data.

12. (currently amended) A selector ~~(60; 70)~~ having multiple channels, logic ~~(62, 64; 72, 73, 74)~~ for selecting a subset of said channels for further processing, and apparatus ~~(2)~~ associated with each of said channels for determining the quality of a digital signal ~~(S)~~, comprising:

a sampler ~~(10)~~ using clock cycles ~~(CLK)~~ for sampling the digital signal ~~(S)~~ with a number n of samples per defined pulse width, ~~whereby~~ where $n \geq 1$;

an edge detector ~~(20)~~ for detecting an edge of a pulse of the sampled digital signal;

a counter ~~(30)~~ for counting the clock cycles between edges detected by the edge detector; and

a deviation detector ~~(40)~~ being able to compare the counted clock cycles ~~(EEC)~~ with a prestored reference-value ~~(EEC_0)~~ in order to provide a deviation value ~~(RJ)~~ as a measure for the instantaneous quality of the digital signal ~~(S)~~;

wherein the logic comprises a minimum detector for detecting a digital signal with the best signal quality measure and a primary multiplexer for selecting the digital signal for further processing.

13. (canceled)

14. (currently amended) A selector having multiple channels, logic for selecting a subset of said channels for further processing, and apparatus associated with each of said channels for determining the quality of a digital signal, comprising:

a sampler using clock cycles for sampling the digital signal with a number n of samples per defined pulse width, whereby $n \geqq 1$;

an edge detector for detecting an edge of a pulse of the sampled digital signal;

a counter for counting the clock cycles between edges detected by the edge detector; and

a deviation detector being able to compare the counted clock cycles with a prestored reference-value in order to provide a deviation value as a measure for the instantaneous quality of the digital signal;

~~Selector (70) according to claim 12~~ wherein the logic ~~(72, 74)~~ comprises a minimum-maximum detector ~~(72)~~ for detecting a first digital signal with the best signal quality measure ~~(PCS)~~ and a second digital signal with the second-best quality measure ~~(DCS)~~ and a diversity multiplexer ~~(74)~~ for selecting these digital signals ~~(PCS, DCS)~~ for further processing.

15. (currently amended) <u>A selector</u> ~~Selector~~ (70) according to claim 14, wherein the logic (73) comprises a channel quality comparator (73) for providing a control signal (ECF).

16. (currently amended) A receiver system ~~(80)~~ including a channel multiplexer ~~(70)~~ having logic ~~(72)~~ including a minimum-maximum detector ~~(72)~~ for detecting a first digital signal with best signal quality measure ~~(PCS)~~ and a second digital signal with second-best quality measure ~~(DCS)~~ and a diversity multiplexer ~~(74)~~ for selecting these digital signals ~~(PCS, DCS)~~ for further processing and a channel detector ~~(101)~~ for determining a pulse position that bases on the first digital signal with the best signal quality measure ~~(PCS)~~ and the second digital signal with the second-best signal quality measure ~~(DCS)~~, the apparatus comprising:

a first storage unit ~~(102)~~ for storing at least one symbol of the first digital signal with the best signal quality measure ~~(PCS)~~;

a second storage unit (104) for storing at least one symbol of the second digital signal with the second-best signal quality measure (DCS); and

a determination unit ~~(118)~~ comprising a probability table ~~(110)~~, which in case that the first and second digital signals ~~(PCS, DCS)~~ are received<u>,</u> is addressed with the at least one symbol of the first digital signal with the best signal quality measure ~~(PCS)~~ and the at least one symbol of the second digital signal with the second-best signal quality measure ~~(DCS)~~, thereby providing a value that is defined as the pulse position ~~(DDS)~~.

17. (currently amended) A method ~~Method~~ for determining the quality of a digital signal ~~(S)~~, ~~the method~~ comprising ~~the steps of~~:

sampling the digital signal ~~(S)~~ with a number n of samples per defined pulse width, ~~whereby~~ where $n \geqq 1$;

detecting an edge of a pulse of the sampled digital signal;

counting the clock cycles between edges; ~~and~~

comparing the counted clock cycles ~~(EEC)~~ with a prestored reference-value ~~(EEC_0)~~ in order to output a deviation value ~~(RJ)~~ as a measure for the instantaneous quality of the digital signal ~~(S)~~; and

feeding the deviation value to an absolute-value limiter unit that provides an absolute deviation value and feeding the absolute deviation value to a storage latch that outputs the absolute deviation value for further processing.

18. (canceled)

19. (original) Method according to claim 18 further comprising the step of feeding the absolute deviation value (PJ) to a leaky integrator (50) that outputs a signal quality measure (J).

20. (original) Method according to claim 17 further comprising the step of detecting a first digital signal having the best signal quality measure (PCS) and selecting it for further processing.

21. (original) Method according to claim 20 further comprising the step of detecting a second digital signal having the second-best signal quality measure (DCS) and selecting these signal (PCS, DCS) for further processing.

22. (original) Method according to claim 17, wherein the quality of the digital signal (S) is determined within the preamble of the digital signal (S).

23. (original) Method according to claim 21, wherein selecting the first digital signal (PCS) and the second digital signal (DCS) stops if the start of a symbol within the preamble of the digital signal (S) has been recognized, then the selection of the first digital signal (PCS) and the second digital signal (DCS) are retained.

24. (original) Method according to claim 17, wherein the deviation value (RJ) and/or the signal quality measure (J) are/is determined for at least two digital signals, preferably for three digital signals.

25. (currently amended) A method for determining quality of a digital signal ~~(S)~~ comprising:

sampling the digital signal ~~(S)~~ with a number n of samples per defined pulse width, ~~whereby~~ where $n \geq 1$;

detecting an edge of a pulse of the sampled digital signal;

counting the clock cycles between edges; ~~and~~

comparing the counted clock cycles ~~(EEC)~~ with a prestored reference-value ~~(EEC~~$_{0}$~~)~~ in order to output a deviation value ~~(RJ)~~ as a measure for the instantaneous quality of the digital signal ~~(S)~~; and

further comprising the following steps for determining a pulse position for the digital signal ~~(S)~~, which is received as at least the first digital signal ~~(PCS)~~ and the second digital signal ~~(DCS)~~:

storing a probability table ~~(110)~~;

storing at least one symbol of the first digital signal ~~(PCS)~~;

storing at least one symbol of the second digital signal ~~(DCS)~~; and

addressing the probability table ~~(110)~~ with the at least one symbol of the first digital signal ~~(PCS)~~ and the at least one symbol of the second digital signal ~~(DCS)~~, ~~thereby~~ whereby the probability table ~~(110)~~ provides ~~providing~~ a value that is defined as the pulse position ~~(DDS)~~.

26. (currently amended) The receiver of claim 16, wherein the logic ~~(72, 74)~~ comprises a channel quality comparator ~~(73)~~ for providing a control signal ~~(ECF)~~.